

METHOD FOR DRIVING A SEMICONDUCTOR SWITCH AND CIRCUIT
CONFIGURATION WITH A SEMICONDUCTOR SWITCH

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Background of the Invention:

Field of the Invention:

The invention relates to a method for driving a semiconductor switch with load current limitation and thermal protection, whose maximum load current is limited and which switches off when a predetermined upper temperature is exceeded and switches on again when the temperature falls below a predetermined lower temperature, and to a circuit configuration with a thermally protected semiconductor circuit.

Semiconductor switches for load switching, i.e. for applying a load which is connected in series with the load path of a semiconductor switch to a supply voltage, are utilized in a wide variety of fields, among them the automotive field. In some of the known commercial semiconductor switching modules, in addition to the actual semiconductor switch, for instance a power MOSFET or power IGBT, there are protective circuits for guarding the semiconductor switch against overload, particularly against excessive temperature or excessive load current, integrated therein. Such switching modules are known

to the person skilled in the art as smart power switches or smart power ICs.

A known technique for protecting the semiconductor switch or other circuit parts in such integrated circuits from excess temperature is to integrate a temperature sensor into the switching module and to evaluate a signal that is delivered by the temperature sensor. If the temperature exceeds a predetermined threshold value, the power transistor is shut off by a protective circuit in order to lower the power consumption of the power module and prevent further heating of the power module. As to the reactivation of the power transistor following such a temperature-related deactivation, there is a distinction between switching modules in which the reactivation is dependent on an external command (latch principle) and those in which it occurs automatically once the switching module cools below a predetermined temperature (restart principle). The advantage of the restart principle is that the switching module reactivates - i.e. returns to the previous operating mode - after cooling, without requiring any external outlay. The disadvantage of the restart principle is that, if the circuit module is overheating due to a shorting of the load, the power transistor is switched on again in short-circuit conditions again, with the result that the temperature in the switching module rises again owing to the large amount of power that gets converted in the switching

module as a consequence of the short, until the upper temperature threshold is reached again and the power transistor is consequently deactivated again. In a switching module with load current limitation, the load current
5 constantly reaches the maximum upper temperature limit under these operating conditions.

The average power that is converted into heat in the semiconductor module during a short can be reduced when the
10 overcurrent limiting begins with smaller currents and therefore limits the maximum load current to lower values. However, it must be taken into account that these switching modules are frequently employed for switching capacitive loads of lamps or electromotors, which have a relatively high
15 initial current that must never lead to the semiconductor switch being turned off as if a failure were occurring. For example, in automotive applications, a basic limiting of the maximum allowable temperature to a lower value is constrained by the fact that temperatures of up to 150° C arise in
20 switching modules there during normal operation, which must not bring about a temperature-related shutdown.

Summary of the Invention:

It is accordingly an object of the invention to provide a
25 method for driving a semiconductor switch and a circuit configuration which overcome the above-mentioned disadvantages

of the prior art methods and devices of this general type, with which the power that is converted into heat in the event of a load short in the semiconductor switch is reduced compared to conventional semiconductor switches.

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With the foregoing and other objects in view there is provided, in accordance with the invention, a method for driving a semiconductor switch having load current limiting and thermal protection. A maximum load current is limited and the semiconductor switch switches off upon a predetermined upper temperature being exceeded and switches on again when a chip temperature falls below a predetermined lower temperature. The method includes operating the semiconductor switch in a normal mode or a fault mode, operating the semiconductor switch in the fault mode upon exceeding the predetermined upper temperature, and limiting a load current to a first maximum value in the normal mode and to a second maximum value, being lower than the first maximum value, in the fault mode.

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The inventive method for driving the semiconductor switch with load current limitation and thermal protection whose maximum load current is limited, which is switched off when a predetermined upper temperature is exceeded and switched on again when the temperature falls below a predetermined lower temperature, provides that the semiconductor switch be

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operated in a normal mode and a fault mode. The semiconductor switch is operated in the fault mode once the temperature rises above the predetermined upper temperature, the difference between the normal and fault modes being the maximum load current at which the current limiting begins. In the normal mode, the load current is limited to a first maximum value, and, in the fault mode, the load current is limited to a second maximum value which is lower than the first.

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The lower of these two load current limit values, which pertains to the fault mode, is selected so that the loads with the lowest impedance for which the semiconductor switch is specified can still be supplied.

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Regardless of the operating mode, the semiconductor switch is switched on again when the temperature drops below a lower threshold value.

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In this method, given a persistent short, a lower maximum current flows through the semiconductor switch during the fault mode than during the normal mode. The circuit configuration with the semiconductor switch is thus heated more slowly and gently, which reduces the temperature-related stress in the semiconductor material and the surrounding housing.

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When in the fault mode, the semiconductor switch is switched off upon exceeding a second upper temperature which is lower than the first upper temperature. As a result, a temperature-related deactivation occurs at lower maximum temperatures than in normal mode. As a result, the semiconductor switch, or an integrated circuit in which the semiconductor switch is integrated, is likewise under a lower temperature-related stress in the event of a fault, i.e. given a short of the load or an overload.

According to the inventive method, the voltage across the load path of the semiconductor switch is also evaluated, the semiconductor switch being operated in the normal mode again, after a transition into the fault mode, when the voltage across the load path of the semiconductor switch has dropped below a predetermined threshold value. The dropping of the load path voltage indicates that the voltage across the load has increased, which indicates that the short that constituted the fault has ended.

The inventive circuit configuration contains a semiconductor switch with an drive terminal and a load path, a protective circuit that is connected to the drive terminal of the semiconductor circuit, a load current sensor that provides a load current signal, and a temperature sensor that is disposed

in the region of the semiconductor switch and provides a temperature measuring signal, the temperature signal and the load current signal being supplied to the protective circuit. In the protective circuit, a first and a second overcurrent
5 signal are available, the protective circuit being capable of assuming a first or second switching state, and, depending on the state, the protective circuit switches off the semiconductor switch in accordance with a comparison of the current signal with the first overcurrent signal or in
10 accordance with a comparison of the current signal with the second overcurrent signal.

There are also first and second overtemperature signals available in the protective circuit, whereby, depending on the
15 state, the protective circuit drives the semiconductor switch into a blocking state in accordance with a comparison of the temperature signal with the first overtemperature signal or in accordance with a comparison of the temperature signal with the second overtemperature signal.

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The circuit configuration advantageously contains a voltage measuring configuration for detecting a load path voltage of the semiconductor switch, which provides a voltage measuring signal which is supplied to the protective circuit, the
25 circuit assuming one of the two switching states depending on the voltage measuring signal.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

5 Although the invention is illustrated and described herein as embodied in a method for driving a semiconductor switch and a circuit configuration with a semiconductor switch, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made
10 therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages
15 thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

20 Fig. 1 is a block diagram of a circuit configuration with a semiconductor switch and a control circuit according to the prior art;

Figs. 2A-2D are graphs showing selected measurement values of
25 the semiconductor switch in a drive method according to the prior art;

Figs. 3A-3D are graphs showing selected measurement values of the semiconductor switch for illustrating a first embodiment of a method for driving the semiconductor switch according to
5 the invention;

Figs. 4A-4D are graphs showing selected measurement values of the semiconductor switch for illustrating a second embodiment of a method for driving the semiconductor switch according to
10 the invention;

Fig. 5 is a circuit diagram of a first exemplifying embodiment of an inventive circuit configuration with the semiconductor switch; and

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Fig. 6 is a circuit diagram of a second exemplifying embodiment of the inventive circuit configuration with the semiconductor switch.

20 Description of the Preferred Embodiments:

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof,
25 there is shown a schematic representation of the structure of a conventional switching module with a power transistor D

whose drain-source path is connected in series with a load, the series circuit with the power transistor and the load being connected between a terminal for supply potential V_{bb} and a terminal for a reference potential GND. The switching

5 module contains a temperature sensor 1 in the region of the power transistor T, which supplies a temperature signal TS to a protective circuit, which shuts off (blocks) the power transistor T given excess temperature. The switching module further contains a current sensor 2, which detects a load

10 current I_{ds} through the power transistor T and supplies a current signal IS to the protective circuit. The current sensor 2 is schematically connected in series with the load in Fig. 1 but can be configured any other way. For instance, the current sensor can function according to the current sense

15 principle, according to which the load current through a cellular transistor is detected by detecting the current through cells parallel to the cells that are passed by the load current.

20 The functioning of such a switching module given the occurrence of a short circuit in the load will be briefly elaborated in connection with Figs. 2A-2D. Figs. 2A-2D represent time curves of the chip temperature, or rather a temperature signal TS that is dependent on the chip

25 temperature, the load current I_{ds} , a voltage U_{ds} across the load path D-S of the power transistor T, and the power P that

is converted into heat in the power transistor. The representation according to Figs. 2A-2D is based on the assumption that a short occurs in the load at time t_{10} . At this instant, the voltage U_{ds} across the load path D-S rises abruptly approximately to the value of the supply voltage V_{bb} . The load current I_{ds} through the power transistor rises with corresponding steepness until it attains the upper limit value. As a result of the voltage rise and the current rise, the power P that is converted into heat in the power transistor also rises steeply, which leads to heating of the power module, which is typically constructed as an integrated circuit. In order to limit the load current in the event of a short, the power transistor T is reset as soon as the load current I_{ds} exceeds a predetermined current threshold I_{ds1} for the purpose of limiting the maximum load current I_{ds} to a value in the region of this current threshold I_{ds1} .

If the chip temperature exceeds an upper temperature threshold T_{So} as a result of the short circuit, the power transistor T is blocked by the protective circuit, as a result of which the load current I_{ds} , and with it the power P that gets converted into heat, drop to zero, as represented at time t_{20} . As a result of the deactivating of the power transistor, the temperature of the module drops until it falls below a lower temperature threshold T_{Su} at time t_{30} and the power transistor is automatically switched on again. As long as the short

still exists, the load current I_{ds} rises steeply again, dropping to zero again as a result of the blocking of the power transistor D only when the chip temperature T_{So} rises above the upper temperature threshold value. The repeated
5 actuating under short conditions leads to degenerative effects in the module as a result of the high currents and the related high temperatures and particularly the high temperature gradients, which effects harm the semiconductor chip itself as well as its housing and thus impair the lifetime of the
10 modules or at least the stability of their operating parameters.

Figs. 3A-3D show the time characteristic of selected measurement values of the semiconductor switch T or a circuit
15 configuration with the semiconductor switch T in an embodiment of a method for driving the semiconductor switch according to the invention. Figs. 3A-3D shows the time characteristics of the chip temperature or a temperature signal T_S that is directly related to the chip temperature, the load current
20 I_{ds} , the load path voltage U_{ds} , and the power P that is converted into heat in the semiconductor switch T.

The signal curve represented in Figs. 3A-3D is based on the assumption that the semiconductor switch T is operated without
25 a fault until time t_1 . At time t_1 a short circuit occurs in a load that lies in series with the semiconductor switch, as a

result of which the load current I_{ds} through the semiconductor switch rises steeply. With the load current, the power that is converted into heat in the semiconductor switch also rises, and with that the chip temperature in the semiconductor body in which the semiconductor switch is integrated. The semiconductor switch is operated with a current limitation; that is, the maximum load current cannot exceed an upper threshold IS_1 even in the event of a short of the load; that is to say, upon the crossing of the upper threshold value, the load current is reset to the threshold value IS_1 by the opening of the semiconductor switch, as can be seen in the current curve between times t_1 and t_2 .

In the inventive method, the semiconductor switch is turned off when the chip temperature exceeds the upper maximum value, i.e. when the temperature signal TS that is dependent on the chip temperature exceeds an upper maximum value TS_1 , as occurs at time t_2 . With the opening of the semiconductor switch T , the load current I_{ds} and the power P that is converted into heat in the semiconductor switch T return to zero.

With the opening of the semiconductor switch due to exceeding the upper maximum value TS_1 , the semiconductor switch transitions into a fault mode in which the semiconductor switch is subsequently driven. The fault mode differs from

the normal mode based on a lower limit value for the maximum allowable load current, which is explained below.

When the temperature measurement value TS falls below a lower
5 threshold value TS3 at time t3, the semiconductor switch T is
switched on again, whereupon the maximum allowable load
current is limited to a second maximum value IS2 which is
lower than the first maximum value IS1. The effect is that,
if there is still a short of the load, less power P is
10 converted into heat in the semiconductor switch T owing to the
low maximum current, and the chip temperature rises more
slowly, the semiconductor switch being switched off again when
the temperature signal TS exceeds the upper maximum value TS1
during fault mode also, as is the case at time t4, for
15 example.

The semiconductor switch is driven in the normal mode again
only when there is no longer a short in the load. In order to
detect this, the voltage Uds across the load path of the
20 semiconductor switch T is detected. During the short,
approximately the entire supply voltage Vbb across the series
circuit containing the semiconductor switch and the load drops
across the load path of the semiconductor switch T. After the
elimination of the short, the load path voltage Uds drops
25 substantially, because the majority of the voltage is across
the load again. An embodiment of the invention therefore

provides that the load path voltage U_{ds} is monitored, and that the semiconductor switch T is driven in the normal mode again — i.e. the load current is limited to the higher value IS_1 — once the load path voltage U_{ds} drops below a predetermined threshold value during fault mode, which is represented in Fig. 3C at time t_5 .

Figs. 4A-4D show time curves of the measurement values that were described in connection with Figs. 3A-3D, in an embodiment of the inventive method in which not only the maximum allowable load current I_{ds} is limited to a lower value IS_2 during fault mode, but also the maximum allowable temperature is limited to a lower temperature, which is represented by a temperature signal TS_2 . Like in the method according to Figs. 3A-3D, in the method according to Figs. 4A-4D the semiconductor switch switches over to fault mode at time t_2 , at which the temperature signal TS_1 which is dependent on the chip temperature crosses beyond the first maximum temperature value TS_1 , whereupon the semiconductor switch is switched off at the time t_2 . The semiconductor switch is switched on again when the chip temperature falls below a lower limit value TS_3 as represented at time t_3 . If there is still a short in the load, the chip temperature then rises again, but the temperature rise is slowed, because the maximum allowable load current is limited during fault mode to

a value IS_2 that is lower than the value IS_1 that is critical during normal mode.

Furthermore, during the fault mode, the semiconductor switch
5 is switched off again once the temperature measuring signal TS rises to a second maximum value TS_2 that is smaller than the first maximum value TS_1 . The effect of the load limitation to the lower value IS_2 during fault mode is that less power is converted into heat in the on state of the semiconductor
10 switch. The effect of the temperature limitation to the lower value TS_2 is that the on-times during fault mode are shorter, and the chip with the semiconductor switch is not heated as strongly.

15 From time t_4 , the semiconductor switch is driven in the normal mode again, in which the load current limitation is based on the higher limit value IS_1 and the temperature limitation is likewise based on the higher limit value TS_1 , once the load path voltage U_{ds} falls below a predetermined
20 limit value indicating that the short has ended.

Fig. 5 represents a first exemplifying embodiment of an inventive circuit configuration with the semiconductor switch T , in this case an n-channel MOSFET, whose drain-source path
25 is connected in series with a load, there being a supply voltage V_{bb} pending across the series circuit of the

semiconductor switch T and the load. The semiconductor switch T is integrated in a semiconductor module, for example, a source terminal S of the semiconductor switch T in this case forming an output terminal AK of the semiconductor module for
5 connecting the load.

The semiconductor switch T conducts and blocks according to a drive signal IN' at its gate terminal G, which is provided by a known driver circuit. The driver circuit contains a charge
10 pump for producing a drive potential that is suitable for driving the semiconductor switch T, which serves as a high-side switch, into a conductive state.

The circuit configuration further contains a protective
15 circuit 20, which protects the semiconductor switch T from a temperature overload and a current overload. A temperature signal TS is supplied to the protective circuit 20, which signal is provided by the temperature sensor 10 that is disposed in the region of the semiconductor switch T as
20 represented in Fig. 5. Technologically, the temperature sensor 10 is advantageously integrated in the same semiconductor body in which the semiconductor switch T is also integrated, specifically in the cell field of the generally cellular semiconductor switch.

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For detecting the load current I_{ds} through the semiconductor switch T, a current sensor 40 is provided, which is connected in series with the load path D-S of the semiconductor switch T in the exemplifying embodiment according to Fig. 5. The
5 current sensor 40 can be realized in any form. Particularly, the current sensor 40 can be realized according to what is known as the current sense principle; i.e., some of the cells of the cellular semiconductor switch T can be used for the current detection. The current sensor 40 provides a current
10 signal IS which is also fed to the protective circuit 20.

The protective circuit 20 is constructed for turning off (blocking) the semiconductor switch T when the temperature signal TS exceeds an upper maximum value. The protective
15 circuit 20 is also configured to drive the semiconductor circuit T such that the load current I_{ds} is limited to a maximum value.

The protective circuit 20 has a control loop with an
20 operational amplifier OPV and a transistor 26 provided for regulating the load current. The transistor 26 is connected between the gate terminal G and the source terminal S of the semiconductor switch T. The transistor 26 is driven by the operational amplifier OPV in dependence on a comparison of the
25 current measurement signal IS with a first or second current limit value IS1, IS2, the first and second current limit

values IS1, IS2 being available in the protective circuit 20 and stored in storage devices 25, 27, for example. In the represented exemplifying embodiment, the first current limit value IS1 or the second current limit value IS2 is supplied to the minus input of the operational amplifier OPV depending on a setting of switch 29, for the purpose of comparing the current measurement value IS with one of these two current limit values IS1, IS2 and driving the transistor 26.

10 If the current measurement value IS exceeds the limit value IS1, IS2 presently applied at the operational amplifier OPV, the operational amplifier OPV drives the transistor 26 to shut down the power transistor T so that the load current Ids is limited.

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The thermal protective circuit contains an additional transistor 26' whose drain-source path is also connected between the gate terminal G and the source terminal S of the power transistor T, and which is driven by a comparison

20 circuit 24 that is supplied with the temperature measuring signal TS and a first upper temperature limit value TS1 and a lower temperature limit value TS3. The comparison circuit 24 is configured to drive the transistor 26' into a conductive state in order thereby to block the semiconductor switch when the temperature signal TS exceeds the upper limit value TS1, and to block the transistor 26', thereby making it possible to

drive the semiconductor switch T into a conductive state based on the input signal IN, when the temperature signal TS falls below the lower temperature limit TS3. To that end, the comparator configuration 24 contains first and second
5 comparators K1, K2, the upper temperature signal TS1 being supplied to the minus input of the first comparator K1, and the lower temperature limit signal TS3 being supplied to the plus input of the second comparator K2. The temperature measuring signal TS is supplied to the respective other inputs
10 of the comparators K1, K2.

The transistor 26' is driven by an RS flip-flop FF1, a set input S of the flip-flop FF1 being supplied with an output signal of the first comparator K1, and the reset input R of
15 the flip-flop FF1 being supplied with the output signal of the second comparator K2. The flip-flop FF1 is set for the purpose of driving the transistor 26' into a conductive state when the temperature signal TS exceeds the upper temperature limit signal TS1, and the flip-flop FF1 is reset for the
20 purpose of blocking the transistor 26' again when the temperature limit signal TS subsequently falls below the lower temperature limit signal TS3.

Depending on which current limit value IS1, IS2 is applied for
25 load current limitation, the protective circuit 20 is operated in a first mode, henceforth a normal mode, or a second mode,

henceforth a fault mode. The normal mode is characterized by the application of the first current limit signal IS1, which is larger than the second current limit signal IS2, for load current limitation.

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The switch 29 across which one of the two current limit signals IS1, IS2 is supplied to the operational amplifier OPV, is driven by a second RS flip-flop FF2, whose switch state determines the operating mode of the protective circuit 20.

10 When the flip-flop FF2 is in reset position, the protective circuit 20 functions in the normal mode, and the switch 29 is in a position in which the first current limit signal IS1 is fed to the operational amplifier OPV. When the flip-flop FF2 is in set position, the protective circuit is in fault mode,
15 and the second current limit signal IS2 is fed across the switch 29 to the operational amplifier OPV for the load current limitation of the semiconductor switch T. The flip-flop FF2 is set when, according to the output signal of the comparator K1, the temperature signal TS exceeds the value of
20 the upper temperature limit signal TS1, the temperature limit signal TS1 being selected such that the temperatures corresponding to the limit signal TS1 are only reached in the event of a fault, for instance when a short occurs in the load. The protective circuit 20 thus changes over into fault
25 mode when the temperature exceeds a limit value defined by the upper temperature signal TS1, the load current being limited

during fault mode to a lower value that is defined by the second current limit signal IS2.

Fig. 6 represents a modification of the circuit configuration represented in Fig. 5, a second temperature limit signal TS2 being available in the protective circuit 20 in this embodiment in addition to the first temperature limit signal TS1, the temperature limit signals TS1, TS2 being stored in storage devices 21, 22. The second temperature limit signal TS2 is lower than the first temperature limit signal TS1. The two temperature limit signals TS1, TS2 are fed to the comparator K1 according to the setting of a switch 28, which, like the switch 29, is driven by the second flip-flop FF2. The switch status of the flip-flop FF2 and the setting of the switch 28 are tuned to one another in such a way that, in normal mode, i.e. when the flip-flop FF2 is in reset position, the first temperature limit signal TS1 is fed to the comparator K1 in order to block the semiconductor switch T if the temperature signal TS should exceed the first temperature limit signal TS1. When the flip-flop FF2 is in set position, the protective circuit 20 is in the fault mode, and the second temperature limit signal TS2 is fed to the comparator K2 across the switch 28, so that during the fault mode it blocks the semiconductor switch T once the temperature signal TS exceeds the second temperature limit signal TS2. In the circuit configurations according to Figs. 5 and 6, in order to

reset the second flip-flop FF2, i.e. to transfer the protective circuit 20 from the fault mode into the normal mode, the load path voltage U_{ds} across the load path D-S of the semiconductor switch T is monitored. The load path voltage U_{ds} is detected by a voltage measuring configuration 20 that provides a voltage measuring signal US. The voltage measuring signal US is compared by a comparator K3 to a voltage reference signal US1 that is available in the protective circuit 20, for instance being stored in a memory 20, and the flip-flop FF2 is reset when the voltage measuring signal US falls below the value of the reference signal US1. A drop in the load path voltage U_{ds} below the reference value US1 indicates the absence of a short of the load, whereas when a short occurred, the temperature rose and the protective circuit 20 was switched into fault mode.